

Regarding the objection to Claims 18 and 22, and the indication of their allowability if re-written in independent form including all of the limitations of the base claim and any intervening claims, Claims 18 and 22 have been so re-written. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 17 and 21 under 35 U.S.C. § 102(b) as allegedly being anticipated by the patent to Lien et al., Claims 17 and 21 have been canceled, thus rendering this rejection moot. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Regarding the rejection of Claims 19, 20, 23 and 24 as allegedly being unpatentable over the patent to Lien, Claims 19, 20, 23 and 24 have been canceled, thus rendering this rejection moot. Wherefore, it is respectfully requested that this rejection be reconsidered and withdrawn.

Attached hereto is Appendix A, which is a marked-up version of the changes made to the claims by the current amendment. The attached Appendix A is captioned "**Version with markings to show changes made.**"

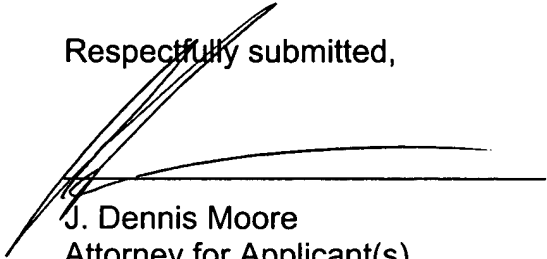
It is respectfully submitted that the claims recite the patentably distinguishing features of the invention and that, taken together with the above remarks, the present application is now in proper form for allowance. Reconsideration of the application, as amended, and allowance of the claims are requested at an early date.

While it is believed that the instant amendment places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, the Applicants petition for an Extension of Time under 37 C.F.R. §1.136. Please charge any fees in connection with the filing of

this paper, including extension of time fees to the Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



J. Dennis Moore  
Attorney for Applicant(s)  
Reg. No. 28,885

Texas Instruments Incorporated  
P.O. Box 655474, MS 3999  
Dallas, TX 75265  
Phone: (972) 917-5646  
Fax: (972) 917-4418

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**In the claims:**

Claim 18 has been amended as follows:

- 1           18. (once amended) An integrated circuit comprising:  
2           a semiconductor substrate;  
3           a first drain region disposed in said substrate;  
4           a first channel region disposed in said substrate directly adjacent to said  
5 first drain region;  
6           a first gate dielectric overlying said first channel region;  
7           a first gate overlying said first gate dielectric;  
8           a first source region disposed in said substrate directly adjacent to said  
9 first channel region;  
10           a second channel region disposed in said substrate directly adjacent to  
11 said first source region and on a side of said first source region opposite to said  
12 first channel region;  
13           a second gate dielectric overlying said second channel region;  
14           a second gate overlying said second gate dielectric;  
15           a second drain region disposed in said substrate directly adjacent to said  
16 second channel region; and [The integrated circuit of claim 17, further  
17 comprising]  
18           an input/output pad electrically coupled to said first gate and to said  
19 second drain region.

Claim 22 has been amended as follows:

- 1           22. (once amended) A method of forming an integrated circuit, said  
2 method comprising:
- 3           forming a first drain region in a semiconductor substrate;
- 4           forming a first source region in said substrate separated from said first  
5 drain region solely by a first channel region;
- 6           forming a second drain region in said substrate separated from said first  
7 source region solely by a second channel region, wherein said second channel  
8 region is a different region than said first channel region;
- 9           forming a first gate dielectric overlying said first channel region and a  
10 second gate dielectric overlying said second channel region;
- 11           forming a first gate overlying said first gate dielectric and a second gate  
12 overlying said second gate dielectric; and [The method of claim 21, further  
13 comprising]
- 14           forming an input/output pad on said semiconductor substrate electrically  
15 coupled to said first gate and to said second drain region.